HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P. O. Box 272400
Fort Collins, Colorado 80528-9599

09-06-00

PATENT APPLICATION

ATTORNEY DOCKET NO. 10992304-1

IN THE U.S. PATENT AND TRADEMARK OFFICE
Patent Application Transmittal Letter

ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

Transmitted herewith for filing under 37 CFR 1.53(b) is a(n): (X) Utility ( ) Design
(X) original patent application,
( ) continuation-in-part application

INVENTOR(S): Alfred I-Tsung Pan

TITLE: Monolithic Common Carrier

Enclosed are:

(X) The Declaration and Power of Attorney. (X) signed ( ) unsigned or partially signed

(X) 3 sheets of drawings (one set) ( ) Associate Power of Attorney

( ) Form PTO-1449 ( ) Information Disclosure Statement and Form PTO-1449

( ) Priority document(s) ( )(Other) _____ (fee $_____)

CLAIMS AS FILED BY OTHER THAN A SMALL ENTITY				
(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) TOTALS
TOTAL CLAIMS	21 — 20	1	X $18	$ 18
INDEPENDENT CLAIMS	2 — 3	0	X $78	$ 0
ANY MULTIPLE DEPENDENT CLAIMS	0		$260	$ 0
BASIC FEE: Design $310.00); Utility $690.00)				$ 690
TOTAL FILING FEE				$ 708
OTHER FEES				$
TOTAL CHARGES TO DEPOSIT ACCOUNT				$ 708

Charge $ 708 to Deposit Account 08-2025. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16, 1.17,1.19, 1.20 and 1.21. A duplicate copy of this sheet is enclosed.

"Express Mail" label no. EL629875815US

Date of Deposit 09/05/00

I hereby certify that this is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231.

By _____

Typed Name: Dee Timmons

Respectfully submitted,

Alfred I-Tsung Pan

By _____

Susan E. Heminger

Attorney/Agent for Applicant(s)
Reg. No. 36,449
Date: 09/05/00
Telephone No.: (650) 236-2738

Rev 12/99 (TransNew)

- Attach as First Page to Transmitted Papers -

APPLICATION

OF

Alfred I-Tsung Pan

FOR

UNITED STATES LETTERS PATENT

ON

MONOLITHIC COMMON CARRIER

Docket No.: 10992304-1

Sheets of Drawings: 3 (Three Sheets)

Patent Agent

Susan E. Heminger

MONOLITHIC COMMON CARRIER

FIELD OF THE INVENTION

The present invention relates generally to precision alignment of integrated circuit devices on a common carrier. More specifically, the present invention relates to precision alignment of integrated circuit devices corresponding to thermal ink jets on a common carrier.

Articles and publications set forth herein are presented for the information contained therein: none of the information is admitted to be statutory "prior art" and we reserve the right to establish prior inventorship with respect to any such information.

BACKGROUND ART

It is well known in the art to use an inkjet printer for applications that require a hardcopy printout on a sheet of media. For example, it is commonplace to use an inkjet printer to print on sheets of paper, transparencies, labels, and the like. In a typical inkjet printer, a carriage holds one or more ink cartridges. Each cartridge has an inkjet printhead (pen) that includes several nozzles from which ink is ejected in a direction that causes the ink to impinge on the sheet of media. Typically, the carriage must travel across the media so that each pen can reach the full area of the media. The media to be printed on is usually driven along a media axis of motion and the pen is driven along a carriage axis of motion that is perpendicular to the media axis. In color inkjet printers, two or more cartridges are needed to print color images. For instance, a color inkjet printer can have four cartridges (black, cyan, magenta, and yellow) with a pen for each color. Consequently, in a four cartridge printer, the carriage must travel the width of the media, plus the width of the four pens, plus the space between pens. Therefore, the width of the inkjet printer is determined to a large extent by the distance the carriage must travel in order to print images on the full area of the media. For example, in an inkjet plotter, the carriage

may have to travel a distance greater than the width of a D-size sheet of media.

Because the carriage must travel across the media, the time it takes to print images includes the travel time for the carriage. Additionally, the mechanical components that move the carriage add to the complexity, size, and weight of the printer and are a source of noise and vibration that can be annoying to a user of the printer.

Moreover, the pens in inkjet printers require periodic alignment to ensure consistent quality in the printed image. Because the pens are mounted in separate cartridges, there is always a risk of misalignment between pens, particularly when one or more cartridges are replaced.

Prior attempts to solve the above mentioned limitations and disadvantages of multiple cartridge inkjet printers include mounting a plurality of inkjet printheads onto a wide substrate such as a multi-layer ceramic substrate or flexible substrate. Those solutions have several disadvantages.

First, expensive precision tooling is required to align the printheads to the substrate. Second, a mismatch between the coefficient of thermal expansion for the printhead and the substrate can result in thermal induced stress on the interconnect used to electrically connect the substrate to the printheads. Additionally, the mismatch can result in misalignment between the substrate and the printheads. Third, the interconnect, the materials used for the substrate, and adhesives used to attach the printheads to the substrate are subject to failures due to the corrosive effects of the ink used in inkjet printers. Forth, the inkjet pens are sensitive to temperature variations caused by waste heat from the printheads. The substrate must have a high thermal conductivity so that the waste heat can be dissipated. If the substrate has a low thermal conductivity, then the waste heat can raise the temperature of the pens resulting in an increase in the pens drop volume. Subsequently, a temperature differential exists among the printheads so that the drop volumes of the printheads can vary depending on their location on the substrate. Ideally, the thermal conductivity of the substrate and the printheads would

be identical so that there is no temperature differential between the printheads resulting in consistent drop volumes among the printheads.

One manner in which multiple printhead alignment can be achieved is described in an application filed by the assignee of the present application. According to this technique, a common carrier substrate is formed having one or more precisely formed pockets. The sides of each pocket are formed to have a side profile that is a near perfect compliment of the side profile of each of a set of fully integrated chips. Due to the complementary side profiles, the chip can be positioned in near perfect self-alignment with all other chips on the substrate. Hence alignment according to this technique is achieved by the precise formation of the pockets and the precise formation of the complimentary edges of the chips.

Therefore, there is a need for a carrier that can mount one or more inkjet printheads in alignment with one another without the need to form precise pockets within the carrier.

SUMMARY OF THE INVENTION

Broadly, the present invention is embodied in a common carrier that includes a carrier substrate for adhering a plurality of unprocessed integrateable chips. Once adhered, the carrier substrate is lithographically processed to form integrated chips that are aligned on the carrier substrate is within lithographic alignment tolerances.

In accordance with one embodiment of the common carrier of the present invention and method of forming thereof, a common carrier is formed to include a plurality of integrated chips and a carrier substrate, where the unprocessed integrateable chip form of the integrated chips are first adhered using a first placement alignment tolerence to the carrier substrate and then are lithographically processed to obtain the plurality of integrated chips on the carrier substrate such that the integrated chips are aligned with each other and the substrate with a second alignment tolerance having lithographic processing precision.

In one embodiment the plurality of integrated chips correspond to a plurality of inkjet printhead IC devices.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a first embodiment of the method of forming a monolithic common carrier.

FIG. 2 shows a second embodiment of the method of forming a monolithic common carrier in which unprocessed, integrateable chips are adhered into slots.

FIG. 3 shows a third embodiment of the method of forming a monolithic common carrier in which unprocessed, integrateable chips are adhered directly onto the surface of a carrier substrate.

FIG. 4 shows a plan view of slots formed into a carrier substrate.

FIGS. 5A and 5B shows a plan view of unprocessed, integrateable chips adhered within the carrier substrate slots.

DETAILED DESCRIPTION

In the following detailed description and in the several figures of the drawings, like elements are identified with like reference numerals.

In general, the present invention is a monolithic common carrier having adhered on its upper surface a plurality of integrated chips, in which the integrated chips are aligned according to lithographic process tolerances. The monolithic common carrier is formed by initially adhering unprocessed integrateable chips to a carrier substrate and then subsequently lithographically processing the chips to form integrated chips on the carrier substrate. As a result, lithographic processing alignment precision is achieved between the integrated chips and between the substrate and the integrated chips. One of the main advantages of this type of formation of a common carrier is that integrated chips formed on the carrier are aligned according to lithographic tolerances without the requirement of a precision placement tool.

It should be noted that for purposes of the present invention an unprocessed, integrateable chip is defined as a workpiece of material which can be lithographically processed to form an integrated device or chip, and which has not yet been exposed to lithographic processing steps. In addition, an integrated device is formed by exposing a workpiece of material to lithographic processing steps to alter the electrical, electro-mechanical, mechanical or physical characteristics of the workpiece.

Fig. 1 shows one embodiment of the method of forming the monolithic common carrier of the present invention including the steps of adhering a plurality of unprocessed, integrateable chips to a carrier substrate using a first placement alignment tolerance (step 10) and lithographically processing the plurality of unprocessed chips to form a plurality of integrated chips (step 11), where the integrated chips are aligned according to lithographic processing tolerances.

Fig. 2 shows a second embodiment of the method of forming the common carrier of the present invention. In this embodiment, a plurality of slots is formed within the upper surface of the carrier substrate (step 12) and a plurality of unprocessed, integrateable chips is adhered into the slots - one chip per slot (step 13). Next, a filler is deposited to fill the gaps formed between the interior edges of the slots and the peripheral edges of the unprocessed chips (step 14). The surface of the carrier substrate is then polished so at to smooth out the surface topology of the carrier substrate such that the top surface of the chips and the carrier substrate are in essentially the same plane (step 15). This step is performed so as to put the carrier substrate in condition for subsequent lithographic processing steps. Next, the unprocessed, integrateable chips are lithographically processed so as to form a plurality of integrated circuit chips on the carrier substrate (step 16). Optionally, if the carrier substrate is embodied as multiple smaller carrier substrates, the carrier substrate can then be separated into individual smaller carrier substrates (not shown in Fig. 2).

In an alternative embodiment of the method (shown in Fig. 3), unprocessed, integrateable chips are adhered directly to the top surface of the carrier substrate instead of into formed slots (step 17) and then the unprocessed chips are lithographically processed to form integrated chips (step 18). In this embodiment, due to the uneven surface of the carrier substrate resulting from adhering the chips *directly* to the upper surface, subsequent processing steps are adapted to account for the uneven topology of the carrier substrate. For instance, after adhering the unprocessed chips to the carrier substrate, the lithographic processing step of depositing photoresist onto the surface of the substrate carrier is performed using curtain or sheet coating, instead of the conventional spin-type photoresist deposition technique. Other alternative lithographic processing steps may be required to account for the uneven topology of the carrier surface.

In one embodiment in which the unprocessed chips are lithographically processed to form integrated circuit devices, conductive nodes or bonding pads are formed on the integrated circuit so as to conductively wire bond the integrated circuit chip to one of another integrated circuit and/or the carrier substrate.

Fig. 4 shows a carrier substrate having a plurality of slots 19 formed into the upper surface 20 of the carrier substrate 21 (Fig. 4). Slot dimensions (i.e., length and width) are designed to be slightly larger than the dimensions (i.e., length and width) of the unprocessed chips to account for placement tool misalignment of the chips. In this embodiment, the placement tool has a tolerance that is significantly less than the lithographic processing steps to be performed in subsequent steps. In one embodiment, the placement tool has a tolerance range of +/- 1 milimeter. The depth of the slots is designed such that the upper surface of the unprocessed chips when adhered into the slot is essentially in the same plane as the upper surface of the carrier substrate.

In accordance with one embodiment of the common carrier, the carrier substrate and the adhesive are composed of a material that has essentially the same coefficient of thermal expansion (CTE) as the unprocessed chips. The reason for the carrier substrate and adhesive having the same CTE as the integrated chips is that in the event of temperature fluctuations, the substrate, adhesive and integrated chips will expand at the same rate, thereby minimizing structural damage to the finished common carrier during periods of temperature fluctuations.

The size of the carrier substrate can be selected dependent on subsequent processing steps for forming the common carrier. For instance, in one embodiment, the carrier substrate size is selected to be adaptable to subsequent lithographic processing steps or equipment used to perform the subsequent lithographic processing steps. Carrier substrate size is also dependent on the number of devices that are to be adhered on it. In one embodiment in which the unprocessed chips are silicon chips, the carrier substrate and adhesive can be composed of polysilicon, glass, metal, ceramic, or similar compositions.

It should be noted that in another embodiment, the size of carrier substrate 21 can be selected so that it can form a plurality of smaller carrier substrates. For example, Fig. 4 shows three carrier substrates 21A (dashed lines). In this embodiment, multiple carrier substrates 21A can be formed simultaneously and then separated in later processing steps. In one embodiment, the adhesive is selected

so as to retain adherence reliability when exposed to subsequent processing steps performed on the common carrier.

Fig. 5A shows the carrier substrate 21 having a plurality of unprocessed, integrateable chips 22 adhered to the carrier substrate within the plurality of slots 19. In one embodiment, a filler is used to fill the gap 23 formed between the interior edge of slot 19 and the peripheral edges of the chip 22 (Fig. 5B). In this way, a relatively continuous top surface is formed on the carrier substrate. In one embodiment, the top surfaces of the unprocessed chips and carrier substrate are polished to even out the common carrier surface topology in order to facilitate subsequent processing steps. In one embodiment, the surface is polished such that the top surfaces of the chips are in the same plane as the top surface of the substrate..

In one embodiment, the filler is selected to have the same or sustantially the same CTE as the integrated chip. In another embodiment, the filler is glass frit.

In one embodiment, the plurality of chips correspond to printhead integrated circuit devices and each of the individual carrier substrates 21A corresponds to a printhead of a single color. In another embodiment, the plurality of chips corresponds to printhead IC devices and each of the individual carrier substrates corresponds to a printhead containing all of the colors for printing for a given printer device.

In still another embodiment of the common carrier of the present invention, the plurality of chips is a component selected from a group consisting of an inkjet printhead, a thermal inkjet printhead, an integrated circuit, an ASIC, a MicroElectroMechanical System, and a fluidic device.

In the preceding description, numerous specific details are set forth, such as specific processing steps and materials in order to provide a through understanding of the present invention. It will be apparent, however, to one skilled in the art that these specific details need not be employed to practice the present invention. In other

instances, well-known lithographic processing steps have not been described in detail in order to avoid unnecessarily obscuring the present invention.

In addition, although elements of the present invention have been described in conjunction with certain embodiments, it is appreciated that the invention can be implement in a variety of other ways. Consequently, it is to be understood that the particular embodiments shown and described by way of illustration is in no way intended to be considered limiting. Reference to the details of these embodiments is not intended to limit the scope of the claims which themselves recited only those features regarded as essential to the invention.

What is Claimed is:

1. A common carrier, comprising:

a carrier substrate having an upper surface; and

a plurality of integrated chips, the integrated chips being first adhered to the upper surface of the carrier substrate in their unprocessed, integrateable chip form according to a placement alignment tolerance and then lithographically processed to form the integrated chips, wherein the integrated chips are aligned according to lithographic alignment tolerance with each other and the substrate.

2. The common carrier as described in Claim 1, wherein the unprocessed integrateable form of the integrated chips are adhered to the carrier substrate using an adhesive which retains adherence reliability when exposed to subsequent processing steps performed on the common carrier.

3. The common carrier as described in Claim 1, wherein the carrier substrate, the adhesive, and the integrated chips have essentially the same coefficient of thermal expansion (CTE).

4. The common carrier as described in Claim 1 wherein the carrier substrate comprises one of polysilicon, glass, metal, and ceramic.

5. The common carrier as described in Claim 1, wherein the carrier substrate includes a plurality of slots for adhering the plurality of chips, one chip per slot.

6. The common carrier as described in Claim 5, wherein the carrier substrate and the integrated chips each have parallel top surfaces which reside essentially within the same plane.

7. The common carrier as described in Claim 6, wherein the upper surface of the carrier substrate and the unprocessed, integrateable form of the integrated chips are polished prior to being lithographically processed.

8. The common carrier as described in Claim 1, wherein the carrier substrate and the integrated chips each have parallel top surfaces which do not reside within the same plane.

9. The common carrier as described in Claim 8, wherein the unprocessed, integrateable chip form of the plurality of chips is lithographically processed using a curtain coating photoresist deposition.

10. The common carrier as described in Claim 7 further comprising a filler material adapted to fill a peripheral gap between the interior edges of each of the slots and the peripheral edges of each of the unprocessed, integrateable form of the integrated chips when each chip is adhered within each slot and prior to being polished.

11. The common carrier as described in Claim 9 wherein the filler material comprises glass frit.

12. The common carrier as described in Claim 1 further comprising:

at least two electrically conductive nodes, the electrically conductive nodes are disposed on either one of the chip and the carrier substrate; and

an interconnect adapted to electrically connect the electrically conductive nodes.

13. The common carrier of Claim 1, wherein the plurality of integrated chips is a component selected from a group consisting of an inkjet printhead, a thermal inkjet printhead, a semiconductor, an integrated circuit, an ASIC, a MicroElectroMechanical System, and a fluidic device.

14. A method of forming a common carrier comprising the steps of:

adhering an unprocessed, integrateable form of a plurality of chips on the upper surface of a carrier substrate according to a first placement alignment precision;

lithographically processing the unprocessed, integrateable form of the plurality of chips to form a plurality of integrated chips on the upper surface, wherein the integrated chips are aligned with each other and the substrate with a second alignment precision having lithographic processing tolerances.

15. The method of forming the common carrier as described in Claim 14 wherein the first alignment precision has a greater tolerance range than the lithographic processing tolerances.

16. The method of forming the common carrier as described in Claim 14 wherein the first alignment precision has a tolerance in the range of +/- 1 milimeter and the second alignment precision has a tolerance in the range of less than 1 micron.

17. The method of forming the common carrier as described in Claim 14 further comprising the steps of:

forming a plurality of slots within the upper surface of the carrier substrate according to the first alignment precision; and

adhering the unprocessed, integrateable form of the integrated chips within the plurality of slots.

18. The method of forming the common carrier as described in Claims 17 further comprising the step of depositing a filler so as to fill a peripheral gap between the interior edges of each of the slots and the peripheral edges of each of the unprocessed, integrateable form of the integrated chips when each unprocessed chip is adhered within each slot.

19. The method of forming the common carrier as described in Claim 18 further comprising the step of polishing the upper surface of the plurality of chips to be in essentially the same parallel plane as the upper surface of the carrier substrate.

20. The method of forming the common carrier as described in Claim 14 further comprising the step of adhering the unprocessed, integrateable form of the integrated chips directly on the upper surface of the carrier substrate such that the upper surface of the unprocessed, integrateable chips is in a parallel, but different, plane than the upper surface of the substrate carrier.

21. The method of forming the common carrier as described in Claim 20 further comprising the step of lithographically processing using curtain coating deposition.

MONOLITHIC COMMON CARRIER

ABSTRACT

A common carrier for forming multiple printheads thereon and method of forming thereof is described. The common carrier includes a carrier substrate for adhering a plurality of unprocessed, integrateable semiconductor chips. Once adhered, the carrier substrate is lithographically processed to form a plurality of integrated circuit (IC) printhead chips such that alignment of the IC chips on the carrier substrate has the precision of lithographic alignment tolerances which is well within printhead alignment requirements.

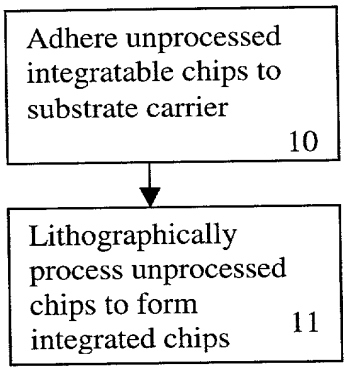

Figure 1

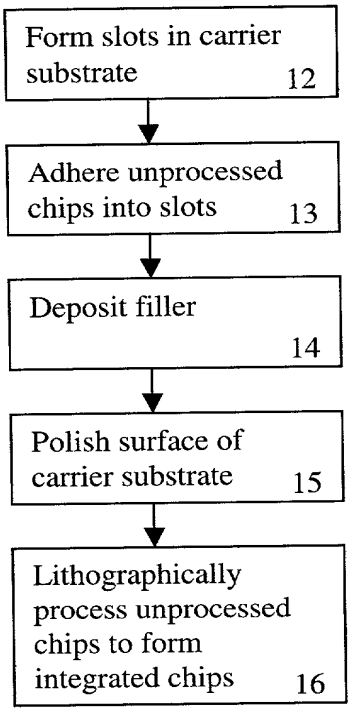

Figure 2

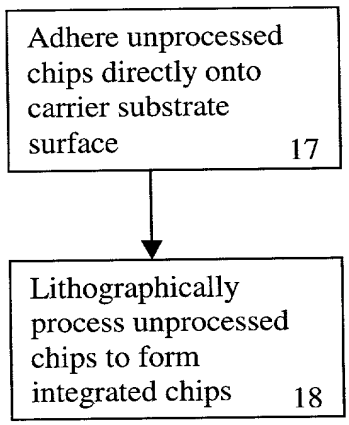

Figure 3

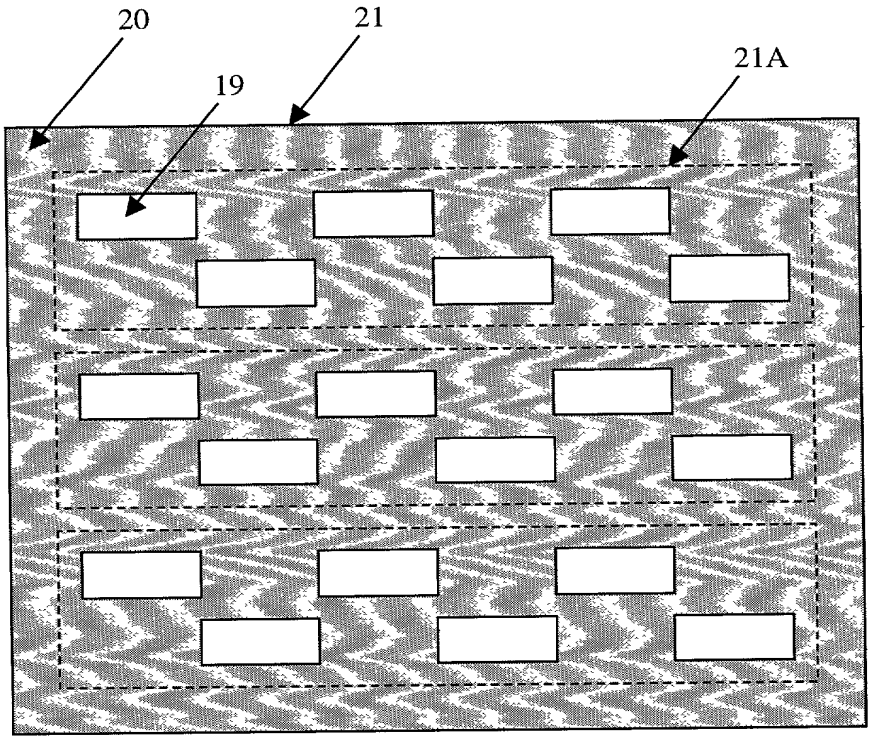

Figure 4

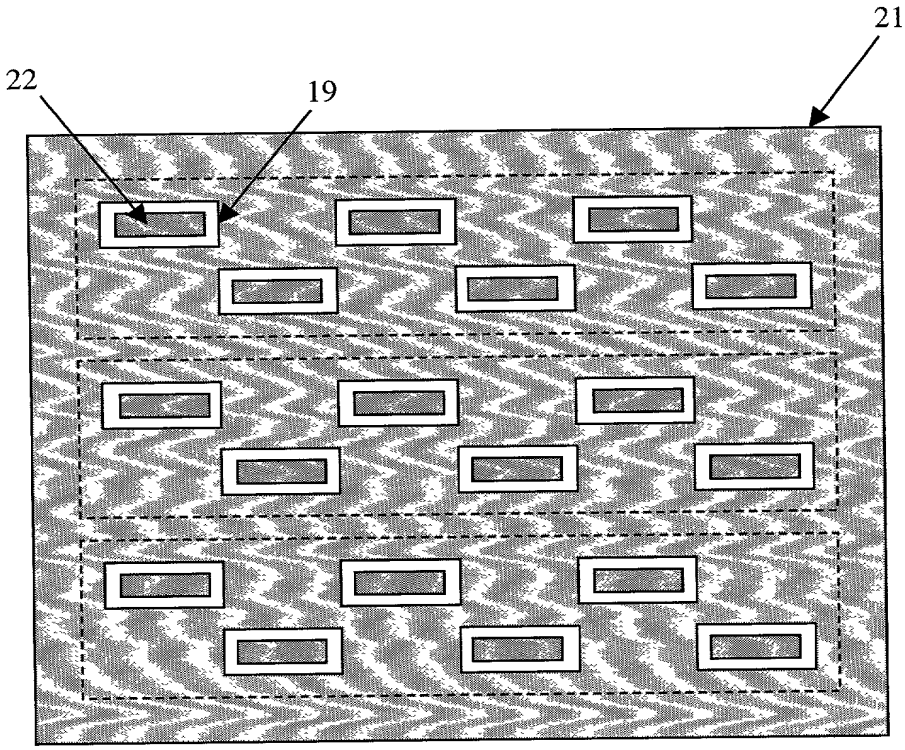

Figure 5A

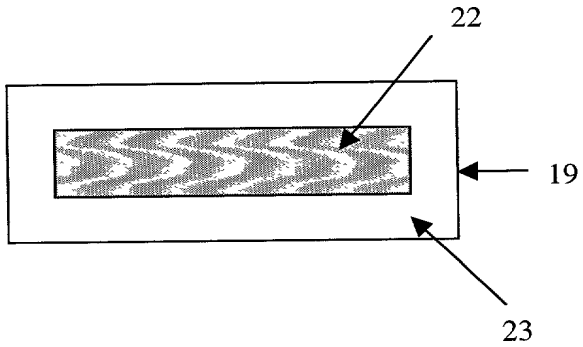

Figure 5B

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

ATTORNEY DOCKET NO. 10992304-1

As a below named inventor, I hereby declare that:

My residence/post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Monolithic Common Carrier

the specification of which is attached hereto unless the following box is checked:

( ) was filed on _____ as US Application Serial No. or PCT International Application Number _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understood the contents of the above-identified specification, including the claims, as amended by any amendment(s) referred to above. I acknowledge the duty to disclose all information which is material to patentability as defined in 37 CFR 1.56.

Foreign Application(s) and/or Claim of Foreign Priority

I hereby claim foreign priority benefits under Title 35, United States Code Section 119 of any foreign application(s) for patent or inventor(s) certificate listed below and have also identified below any foreign application for patent or inventor(s) certificate having a filing date before that of the application on which priority is claimed:

COUNTRY	APPLICATION NUMBER	DATE FILED	PRIORITY CLAIMED UNDER 35 U.S.C. 119
			YES: ___ NO: ___
			YES: ___ NO ___

Provisional Application

I hereby claim the benefit under Title 35, United States Code Section 119(e) of any United States provisional application(s) listed below:

APPLICATION SERIAL NUMBER	FILING DATE

U. S. Priority Claim

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION SERIAL NUMBER	FILING DATE	STATUS (patented/pending/abandoned)

POWER OF ATTORNEY:

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith:

Customer Number 022879

Place Customer Number Bar Code Label here

Send Correspondence to:	Direct Telephone Calls To:
HEWLETT-PACKARD COMPANY **Intellectual Property Administration** **P.O. Box 272400** **Fort Collins, Colorado 80528-9599**	**Susan E. Heminger** **(650) 236-2738**

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Inventor: Alfred I-Tsung Pan **Citizenship:** US

Residence: 1676 Kennard Way Sunnyvale CA 94087

Post Office Address: Same as residence

Inventor's Signature _____ Date Aug 31, 2000